1	S A A A A A A A A A A A A A A A A A A A		J PACKAGE
•	Organization		(TOP VIEW)
•	Single 5-V Power Supply	2	Van 1 ()28 Van
•	Pin Compatible with Existing 64K and 128K EPROMs	4	3 26
	All Inputs/Outputs Fully TTL Compatible	4 4	A6 4 25 A8
•	Max Access/Min Cycle Time '27C128-1, '27C128-15 150 ns '27C128-2, '27C128-20 200 ns		
	'27C128-25 '27C128-30 '27C128-45		× = =
	HVCMOS Technology		02 12 17 06
	3-State Output Buffers	GA	15
	400 mV Guaranteed DC Noise Immunity with Standard TTL Loads		PIN NOMENCLATURE
•	Low Power Dissipation (VCC=5.25 V) Active 210 mW Worst Case Standby 14 mW Worst Case	A0.A13	Address Inputs Chip Enable/Power Down Output Enable
	(CMOS-input Levels)	GND PGM	Ground Program Outputs
		200	5-V Power Supply
		ddy	Aiddoc Jawel Action

description

memories. These devices are fabricated using HVCMOS technology for high speed and simple interfactivith MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TT The TMS27C128 series are 131,072-bit, ultraviolet-light erasable, electrically programmable read-onl circuits without the use of external pull-up resistors, and each output can drive one Series 74 TTL circu without external resistors. The data outputs are three state for connecting multiple devices to a commo bus. The TMS27C128 is pin compatible with existing 28-pin ROMs and EPROMs. It is offered in a dual-ir line ceramic package (J suffix) rated for operation from 0°C to 70°C.

signals are TTL level. For programming outside the system, existing EPROM programmers can be use Locations may be programmed singly, in blocks, or at random. Since these EPROMs operate from a single 5-V supply (in the read mode), they are ideal for use microprocessor-based systems. One other (12.5 V) supply is needed for programming, but all programmir

operation

a single 5-V supply. All inputs are TTL level except for Vpp during programming (12.5 V) and 12 V or There are seven modes of operation for the TMS27C128 listed on the following page. Read mode require A9 for signature mode.

PRODUCTOR DATA decuments contain innormation exercant as a publication data. Products conform to appedications par the terms of laras Instruments atsafers werenty. Production processing does not necessarily include testing of all parameters.

TEXAS INSTRUMENTS

TMS27C128 131,072-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY

switching characteristics over full ranges of recommended operating conditions (see Note 4)

TMS27C128 131,072-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY

PARAMETER	TEST CONDITIONS	'27C128-1	'27C128-2	.27C128	LIND
	ISE HOLES 4 WILL DI	MIN MAX	MIN MAX	MIN MAX	
Access time from address		150	2000		
Access time from chin anable			2007	067	us
000000000000000000000000000000000000000		150	200	250	ns
Output enable time from G	CL = 100 pF,	75	75	1001	1
Output disable time from G or E, whichever occurs first	1 Series 74 TTL Load, Input t _r ≤ 20 ns,	0 60	0 80	0 60	
Output data valid time after	Input ty ≤ 20 ns				
G, whichever occurs first		0	0	0	SC

	PARAMETER	TEST CONDITIONS	'27C128-3	'27C128-4	TINU
1.	Account the fact	6	MIN MAX	MIN MAX	
(a(A)	Access time from address		300	450	SU
(a(E)	Access time from chip enable		300	450	900
en(G)	Output enable time from G	CL = 100 pF,	120	001	28
dis	Output disable time from G or	1 Series 74 TTL Load,		061	Su
	Cutout data valid size effect	Input t _r ≤ 20 ns.	0 105	0 130	us
v(A)	change of address, E, or G, whichever occurs first		0	0	SC

Value calculated from 0.5 V delta to measured output level. This parameter is only sampled and not 100% tested.

recommended timing requirements for programming, $T_A = 25\,^{\circ}\text{C}$, $V_{CC} = 6$ V, $V_{PP} = 12.5$ V (see Note 4)

pulse duration MIN NOM MAX ation 0.95 1 1.05 ation 2.85 78.75 time 2 2 time from \$\overline{G}\$ 0 130 time from \$\overline{G}\$ 2 150 e 2 2 me 2 2 me 2 2 me 0 0				-	
Hintel program puse duration 0.95 1.05	1		MIN NOM MAX		UNIT
Final pulse duration	ŝ	mittal program pulse duration	1	92	SW
Address setup time 2 E setup time 2 G setup time 2 Output disable time from G 0 130 Data setup time 2 150 Vpp setup time 2 2 VCC setup time 2 2 Address hold time 2 2 Data hold time 0 0	Ñ	Final pulse duration	7	36	
E setup time 2 G setup time 2 Output disable time from G 0 130 Output enable time from G 0 130 VPP setup time 2 150 VCC setup time 2 2 Address hold time 2 2 Data shold time 0 0		Address setup time			SE
G setup time 2 Output disable time from G 0 130 Output enable time from G 0 130 Date setup time 2 150 VCz setup time 2 2 Address hold time 2 150 Date hold time 0 150		E setup time	4 6	+	H.S
Output disable time from \$\overline{G}\$ Output enable time from \$\overline{G}\$ Output enable time from \$\overline{G}\$ Output enable time \$\overline{G}\$ Output enable time \$\overline{G}\$ Opp setup time \$\overline{G}\$ Address hold time \$\overline{G}\$ Onte hold time \$G		\$ setup time	, ,	+	trs.
Output enable time from \$\overline{G}\$ 150 Data setup time VCC setup time 2 Address hold time 2 Address hold time 0 Data hold time		Output disable time from G	, ,	9	HS.
Date setup time 2 VPP setup time 2 VCC setup time 2 Address hold time 2 Date hold time 0		Output enable time from G	081	2 9	Sc
Vpp setup time 2 VCC setup time 2 Address hold time 2 Data hold time 0		Data setup time	061	2	SU
V _{CC} setup time 2 Address hold time 0 Data hold time 0	6	Vpp setup time	2 2	+	μS
7 0	0	VCC setup time	7	+	μS
		Address hold time	7	+	μS
		Data hold time		+	hr.S

NOTES: 4. For all switching characteristics and timing measurements, input pulse levels are 0.65 V to 2.2 V and Vpp = 12.5 V ± 0.5 V during programming, Input and output timing reference levels are 0.8 V and 2 V.

5. Common test conditions apply for tgis(g) except during programming.

PARAMETER MEASUREMENT INFORMATION

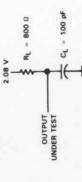


FIGURE 2. OUTPUT LOAD CIRCUIT

OUTPUT tv(A) * ten(G) * ADDRESSES VALID read cycle timing 01.08 10 A0-A13 lw

× ×

VOH Vol

TEXAS INSTRUMENTS

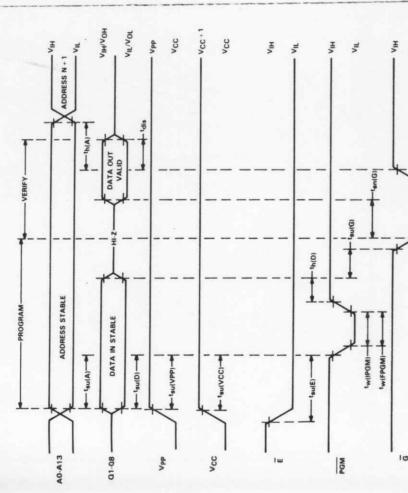
TEXAS INSTRUMENTS

12.5-V Power Supply

SEPTEMBER 1984 - REVISED NOVEMBER 1985

262,144-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY

TMS27C256



Chip Enable/Power Down 28 VCC 27 A14 26 A13 25 A8 24 A9 22 A11 22 D A11 20 E 5-V Power Supply 15 0 05 15 0 05 PIN NOMENCLATURE Address Inputs Output Enable J PACKAGE (TOP VIEW) Outputs 01-08 GND Low Power Dissipation (VCC = 5.25 V) 400 mV Guaranteed DC Noise Immunity All Inputs/Outputs Fully TTL Compatible 170 ns 200 ns 250 ns 300 ns 450 ns Pin Compatible with Existing 128K and -Standby . . . 1.4 mW Worst Case (CMOS-Input Levels) -Active . . . 210 mW Worst Case 170 .27C256-25 Max Access/Min Cycle Time .27C256-17 .27C256-20 .27C256-45 Organization . . . 32K × 8 with Standard TTL Loads Single 5-V Power Supply 3-State Output Buffers **HVCMOS Technology** 256K EPROMs 27C256-1, 27C256-4, 27C256-2, .27C256-3, .27C256,

description

The TMS27C256 series are 262,144-bit, ultraviolet-light erasable, electrically programmable read-only memories. These devices are fabricated using HVCMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three state for connecting multiple devices to a common bus. The TMS27C256 is pin compatible with existing 28-pin ROMs and EPROMs. It is offered in a dual-inline ceramic package (J suffix) rated for operation from 0°C to 70°C.

Since these EPROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (12.5 V) supply is needed for programming, but all programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

operation

7

There are seven modes of operation for the TMS27C256 listed on the following page. Read mode requires a single 5-V supply. All inputs are TTL level except for Vpp during programming (12.5 V) and 12 V on A9 for signature mode.

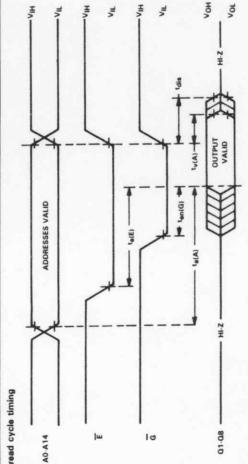
REDUCTION ONTA decements constain information urrant as of publication data. Products conform to appetifications per the terms of Toxas Instruments Istandard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS INSTRUMENTS

99-9

TEXAS INSTRUMENTS

262,144-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY MS27C256



- VERIFY-ADDRESS STABLE PROGRAM

Vcc+1 HON/HIN VIL/VOL VCC VCC NH N 7 ¥ / VPP ADDRESS N+1 tdis DATA OUT (D)ue (D)4) DATA IN STABLE (W(FPGM) (MDdII)M - (d)met -(En(E) # (MAN)ma * tau(VCC) - (au(A) 01.08 10 VPP VCC A0-A14

TEXAS INSTRUMENTS

524,288-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY

PRODUCT PREVIEW

NOVEMBER 1985

(TOP VIEW) J PACKAGE

		FPROMe
		512K
64K×8	r Supply	with Existing 512K F
tion	8 5-V Power	9
Organiza	Single 5	Pin Compatibl
	1	

K EPRO	otible
512K	Comp
Existing	IT All
e with	to E.
Pin Compatible	All lange/Outputs Fully TTI Compatible
Pin	1

	ns	us	ns	US
	200	250	300	
Min Cycle Time	.27C512-20	'27C512-25	'27C512-30	'27C512-45
Max Access/Min Cycle	.27C512-2,	'27C512,	'27C512-3,	'27C512-4,

A15 C 28 VCC A12 27 A14 A7 3 26 A13 A6 4 25 A8 A6 4 25 A8 A6 6 2 24 A9 A7 22 6 VPP A2 8 20 E A1 9 E

HVCMOS Technology

400 mV Guaranteed DC Noise Immunity with Standard TTL Loads • 3-State Output Buffers

Low Power Dissipation (VCC = 5.25 V) -Standby . . . 1.4 mW Worst Case (CMOS-Input Levels) -Active ... 263 mW Worst Case

description

Chip Enable/Power Down

PIN NOMENCLATURE Address Inputs 12.5 V Power Supply

Output Enable

5-V Power Supply

Outputs

01.08

GND

VCC G/Vpp

devices are fabricated using HVCMOS technology for high speed and simple interface electrically programmable read-only memories. These The TMX27C512 series are 524,288-bit, erasable, ultraviolet-light

resistors, and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three state for connecting multiple devices to a common bus. The TMX27C512 is pin compatible with existing 28-pin ROMs and EPROMs. It is offered in a dual-in-line ceramic package (J suffix) rated for operation (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up with MOS and bipolar circuits. All inputs from 0°C to 70°C. Since these EPROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (12.5 V) supply is needed for programming, but all programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

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TEXAS INSTRUMENTS

6-64

program cycle timing